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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

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BRAGDON, REGINALD GLENWOOD	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL K. GSCHWIND and VALENTINA SALAPURA

Appeal 2009-001821
Application 09/940,709
Technology Center 2100

Decided: November 6, 2009

Before JEAN R. HOMERE, JAY P. LUCAS, and JAMES R. HUGHES, *Administrative Patent Judges*.

HUGHES, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) (2006) from the Examiner's rejection of claims 1-37. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' Invention

Appellants[1] invented a configurable memory system within a microprocessor (chip) having multiple modes of operation, including a cache mode and a local memory (non-cache) mode. (Spec. 4, l. 7 to 5, l. 4.)[2]

Claim

Independent claim 1 further illustrates the invention. It reads as follows:

> 1. A memory system on a chip, comprising:
>
> a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory, wherein the configurable memory comprises a memory array in which both tag bits and data bits are stored in a single data line in the memory array, in the first mode of operation.

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[1] The real party in interest is International Business Machines Corp. (App. Br. 1.)

[2] We refer to Appellants' Specification ("Spec."), Appeal Brief ("App. Br.") filed November 5, 2007, and Reply Brief ("Reply Br.") filed March 25, 2008. We also refer to the Examiner's Answer ("Ans.") mailed January 25, 2008.

Reference

The Examiner relies on the following reference as evidence of unpatentability:

Baltz	US 6,321,318 B1	Nov. 20, 2001 (Filed Dec. 15, 1998)
Saulsbury	US 2002/0087821 A1	July 4, 2002 (Filed Mar. 8, 2001)
Sample	US 6,377,912 B1	Apr. 23, 2002 (Filed Aug. 13, 1999)
Isaak	US 6,426,549 B1	July 30, 2002 (Filed Nov. 3, 2000)
Natarajan	US 6,611,796 B1	Aug. 26, 2003 (Filed Oct. 20, 1999)
Kumar	US 6,678,790 B1	Jan. 13, 2004 (Filed June 9, 1997)
Miyake	US 6,868,472 B1	Mar. 15, 2005 (Filed Sept. 28, 2000)

Rejections

The Examiner rejects claim 29 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

The Examiner rejects claims 22-37 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.[3]

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[3] The Examiner rejects claims 22-37 under 35 U.S.C. § 112, first paragraph in the Final Office Action mailed June 4, 2007. The Examiner expressly withdraws the rejection of independent claims 22, 26, 29, and 33 in the

The Examiner rejects claims 1-8 and 10-20 under 35 U.S.C. § 102(e) as anticipated by Kumar.

The Examiner rejects claims 1 and 21 under 35 U.S.C. § 102(e) as anticipated by Saulsbury.

The Examiner rejects claims 1, 10-14, and 21 under 35 U.S.C. § 102(e) as being anticipated by Baltz.

The Examiner rejects claims 1-3, 6-10, 13-17, 20-23, 25, 26, 29, 30, 32, and 33 under 35 U.S.C. § 102(e) as being anticipated by Miyake.

The Examiner rejects claim 24 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Miyake and Sample.

The Examiner alternately rejects claim 24 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Miyake and Natarajan.

The Examiner rejects claims 27, 28, 31, and 34-37 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Miyake and Isaak.

Appellants' Contentions

Appellants contend that claim 29 complies with the written description requirement. (App. Br. 9-11.)

Appellants contend that the subject matter of claims 1-8 and 10-20 is not anticipated by Kumar because the reference does not disclose a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation. (App. Br. 13.)

Answer. (Ans. 3.) We understand the withdrawal to include dependent claims 23-25, 27, 28, 29-32, and 34-37. We will therefore not address Appellant's arguments concerning the withdrawn 35 U.S.C. § 112, first paragraph rejection of claims 22-37, and we will not evaluate the merits of the withdrawn rejection.

Appellants also contend that the subject matter of claims 10-14 is not anticipated by Kumar because the reference does not disclose a configurable memory that is capable of selecting either the first mode of operation or the second mode of operation based upon an address comparison. (App. Br. 15-16.)

Appellants contend that the subject matter of claims 1 and 21 is not anticipated by Saulsbury because the reference does not disclose a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation. (App. Br. 17.)

Appellants contend that the subject matter of claims 1, 10-14, and 21 is not anticipated by Baltz because the reference does not disclose a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation. (App. Br. 18.) Appellants also contend that the subject matter of claims 10-14 is not anticipated by Baltz because the reference does not disclose a configurable memory that is capable of selecting either the first mode of operation or the second mode of operation based upon an address comparison. (App. Br. 18, 15-16.)

Appellants contend that the subject matter of independent claims 1, 22, 26, 29, 30 and 33 is not anticipated by Miyake because the reference does not disclose a configurable memory having a first (cache) mode of operation and a second (local, non-cache memory) mode of operation. (App. Br. 19.) Appellants also contend that the subject matter of claims 22, 26, 29, 30 and 33 is not anticipated by Miyake because the reference does not disclose generating a control signal based on an address comparison of a

supplied address to at least one address range contained in a configuration register to select the first or second mode of operation. (App. Br. 19-20.)

Appellants contend that the subject matter of dependent claims 24, 27, 28, 31, and 34-37, is not rendered obvious by virtue of the dependency of the claims on their respective independent base claims. (App. Br. 21.)

Examiner's Findings and Conclusions

The Examiner finds that each of the claims is properly rejected. (Ans. 3-13.)

Claim Groupings

Based on the Appellants' arguments in the principal Brief on appeal, we find the following claim groupings. Appellants argue independent claim 29 with respect to the written description rejection. Appellants argue independent claim 1 and dependent claim 10 with respect to the § 102(e) rejections over Kumar and Baltz, but do not separately address claims 2-8, 11-14, or 21, which depend on claims 1 and 10, respectively. (App. Br. 15-16, 18.) Appellants argue independent claim 1, but do not separately address dependent claim 21 with respect to the § 102(e) rejection over Saulsbury. (App. Br. 17.) Appellants argue independent claims 1, 22, 26, 29, 30, and 33 with respect to the § 102(e) rejections over Miyake, but do not separately address claims 2, 3, 6-10, 13-17, 20, 21, 23, 25, or 32, which depend on the respective base claims. (App. Br. 19-20.) We address only those arguments that Appellants present in the Brief. Arguments that Appellants could have made but chose not to make in the Brief are waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) ("Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has

grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.").

ISSUES

Based on Appellants' contentions, as well as the findings and conclusions of the Examiner, the issues before us are as follows.

1. Did Appellants establish that the Examiner erred in finding Appellants failed to comply with the written description requirement with respect to claim 29?

2. Did Appellants establish that the Examiner erred in finding Kumar discloses a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation?

3. Did Appellants establish that the Examiner erred in finding Kumar discloses a configurable memory that is capable of selecting either the first mode of operation or the second mode of operation based upon an address comparison?

4. Did Appellants establish that the Examiner erred in finding Saulsbury discloses a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation?

5. Did Appellants establish that the Examiner erred in finding Baltz discloses a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation?

6. Did Appellants establish that the Examiner erred in finding Baltz discloses a configurable memory that is capable of selecting either the first mode of operation or the second mode of operation based upon an address comparison?

7. Did Appellants establish that the Examiner erred in finding Miyake discloses a configurable memory having a first cache mode of operation and a second non-cache mode of operation?

8. Did Appellants establish that the Examiner erred in finding Miyake discloses generating a control signal based on an address comparison of a supplied address to at least one address range contained in a configuration register to select the first or second mode of operation?

FINDINGS OF FACT (FF)

Appellants' Specification

1. Appellants' Specification describes a "memory system" including "a configurable Random Access Memory (RAM) array" with a local, non-cache mode (first mode) of operation and a cache (second mode) of operation. The "configurable RAM array has a memory portion for storing tag bits and data bits in a single logical line in the second mode of operation." (Spec. 5, ll. 5-14.)

2. Appellants' Specification also describes multiple configurable modes of operation as follows:

> These control logic components enable, for example, four modes of operation: local memory read mode; local memory write mode; cache read mode; and cache write mode.

(Spec. 16, ll. 10-13.)

3. Appellants' Specification describes the cache mode of operation as follows:

> When the cache mode configuration is selected by mode selection logic 435, a read operation is performed as follows: the memory address 422 and one or several control signals 424 are input to the configurable memory array 130. The array address mapping module 425 maps the memory address 422 to an array address 432, and the control module 430 generates signals necessary to read data from the addressed memory location. Data read from the memory array 410 are compared for tag match in the tag match logic 440. If a cache hit occurs, then the addressed data are selected using the multiplexer 445, and the result is passed to the memory read data bus 452 by corresponding selection of the multiplexer 450. In the preferred embodiment, cache tags are included in data lines stored in the memory array 410, but alternative implementations can include separate memory arrays for storing data and tags.

(Spec. 17, l. 22 to 18, l. 14.)

Kumar Reference

4. Kumar describes an integrated circuit (chip) with a reconfigurable memory that operates as either on-chip main memory or as on-chip cache. (Col. 2, ll. 33-40.)

5. Kumar describes the reconfigurable memory and its function as follows:

> FIG. 2 illustrates one embodiment of the reconfigurable memory 12 which functions as either a direct-mapped cache memory or a main memory. The reconfigurable memory 12 in this embodiment includes a tag array 50, a data array 52, a row decoder circuit 54, an address register 14, a data buffer 20, a comparator circuit 56, a base address comparator 39, and a control circuit 58.

> The data array 52 includes n rows of memory cells, each row for storing a data line. The data lines in the data array 52 may also be referred to as data blocks or data words. The tag array 50 includes n rows of memory cells for storing sets of tags. Each row of the tag array 50 corresponds to one of the data lines in the data array 52. The tag array 50 and the data array 52 may be implemented as static random access memory (SRAM) cells or dynamic random access memory (DRAM) cells.
>
> The address register 14 holds a physical address which is received via the address bus 22. The physical address held in the address register 14 is used to select rows of the tag array 50 and the data array 52. The physical address in the address register 14 is subdivided into a set of tag bits 42, a set of index bits 40, and a set of offset bits. The offset bits of the physical address in the address register 14 specify subareas, such as bytes or words, of the data lines in the data array 52.
>
> The row decode circuit 54 decodes the index bits 40 held by the address register 14 and drives a set of word lines 60 coupled to the tag array 50 and the data array 52. The particular row of the data array 52 selected by the word lines 60 provides a set of data bits 30 which may or may not be valid. The particular row of the tag array 50 selected by the word lines 60 provides a set of tag bits 32.

(Col. 3, ll. 21-52; Figs. 1(b), 2.)

6. Kumar's reconfigurable memory operates as either on-chip main (local, non-cache) memory or as on-chip cache based on an address comparison and a control signal (cache hit or base address match). (Col. 3, l. 37 to col. 4, l. 12; col. 4, l. 25 to col. 5, l. 26; Figs. 1(b), 2, 3.)

7. Kumar describes the operation of the address comparison and control signal as follows:

> The CPU core 26 may set the cache/main access control bit and load the base address into the control register 16 via control register signal lines 23.

> The CPU core 26 transfers physical addresses via the address bus 22 while fetching either instructions or data. The reconfigurable memory 12 examines the physical addresses carried on the address bus and the control signal 36. The reconfigurable memory 12 drives data onto the data bus 24 in response to valid physical addresses for cached data or valid physical addresses for main memory data depending on the indication carried by the control signal 36.
>
> The reconfigurable memory 12 may also accept as input a base address for the data elements stored in the memory 12. The base address is transferred to the reconfigurable memory 12 via the address lines 37.

(Col. 2, l. 62 to col. 3, l. 10; Figs. 1(b), 2.)

8. Kumar describes the operation of the address comparison and control signal for cache configuration as follows:

> The comparator circuit 56 compares the tag bits 42 from the address register 14 to the tag bits 32 from the tag array 50. The comparator circuit 56 asserts a cache_hit signal 62 if the tag bits 42 match the tag bits 32. The control circuit 58 generates a valid signal 34 in response to the control signal 36 and the cache_hit signal 62. The valid signal 34 enables or disables the data buffer 20.
>
> The control circuit 58 asserts the valid signal 34, thereby enabling the data bits 30 onto the data bus 24, if the control signal 36 indicates that the reconfigurable memory 12 is a cache memory and if the cache_hit signal 62 is asserted to indicate a cache hit.

(Col. 3, ll. 53-64; Figs. 1(b), 2.)

9. The tag bits represent a portion of the address in the address register, i.e., a range of addresses. (Col. 3, ll. 37-45.)

10. Kumar describes the operation of the address comparison and control signal for non-cache memory configuration as follows:

> The address of a data element being accessed from address register 14 is input into the base address comparator 39. The base address 37, from the control register 16 (or 16') and the control signal 36 are also input into the base address comparator 39. If the control signal 36 indicates that the reconfigurable memory 12 is operating in main memory mode, the base address comparator 39 compares the base address 37 to the corresponding address bits of the address 15 and indicates a match on a valid address signal line 41. . . .
>
> In addition, the control circuit 58 asserts the valid signal 34 to enable the data buffer 20 if the control signal 36 indicates that the reconfigurable memory 12 is a main memory and if the valid address signal line 41 indicates that the corresponding bits of address 15 match the predetermined base address of the reconfigurable memory 12.

(Col. 4, ll. 1-18; Figs. 1(b), 2.)

Saulsbury Reference

11. Saulsbury describes an integrated circuit (chip) with an on-chip reconfigurable memory configurable as either physical (non-cache) memory or as cache memory. (¶¶ [0005], [0067].)

12. Saulsbury's reconfigurable memory "comprises DRAM memory [that] can be configured as either cache memory with associated tags or as directly accessible physical memory. Alternatively, memory 14 can be a combination of both cache and physical memory. (¶ [0067].)

Baltz Reference

13. Baltz describes an integrated circuit (chip) with an on-chip reconfigurable memory. A program memory controller (PMC) configures the memory as either cache or non-cache memory. (Abstract; col. 2, ll. 18-26, 38-46; col. 5, ll. 6-35; Figs. 1, 5, 9.)

14. Baltz's PMC (30) includes data RAM (program memory/cache) (31) and tag RAM (32). (Col. 2, ll. 18-26, 38-46; col. 5, ll. 6-35; Figs. 1, 5, 9.) In cache mode, the tag RAM of the program memory controller stores tags corresponding to "each frame in memory 31, in order to track the contents of the cache." (Col. 5, ll. 8-11.) "The eleven-bit block offset [(bits 5-15, Fig. 5)] is used both as an address for the appropriate tag within tag RAM 32 and as an address for the appropriate frame within memory 31. (Col. 5, ll. 11-14.)

15. Baltz's PMC performs an address comparison to determine if valid data is stored in the on-chip memory. (Col. 4, ll. 44-62; col. 5, ll. 6-35.) For example, in memory map mode, "the 64K bytes of on-chip memory may be selected to reside at a contiguous block of memory in address space starting at address 140 0000, as shown in FIG. 4A, or at a starting address of 000 0000, as shown in FIG. 4B." (Col. 4, ll. 58-62.) In cache mode, the PMC divides a provided address "into a ten-bit tag (bits 16-25) and an eleven-bit block offset (bits 5-15)." (Col. 5, ll. 6-8; Fig. 5.) "Each eleven-bit location within tag RAM 32 contains a validity bit and a ten-bit tag." (Col. 5, ll. 14-16.) "[A]s each new fetch packet is requested, its address is partitioned within program memory controller 30 into a compare tag and a block offset. The block offset is used to retrieve a tag from tag ram 32." (Col. 5, ll. 20-24.) "If the tag validity bit of the retrieved tag is set, the

retrieved tag is compared to the compare tag in tag comparator 34 . . . . If the two tags are identical, comparator 34 registers a cache hit . . . ." (Col. 5, ll. 26-32.) "If a cache hit occurs, the requested fetch packet is retrieved from on-chip memory 31 using the block offset as an address." (Col 5, ll. 33-35.)

Miyake Reference

16. Miyake describes an integrated circuit (chip) with a memory configurable either as cache or non-cache RAM memory. (Col. 34, ll. 40-54; col. 36, ll. 38-55; Figs. 35-38, element 320.)

17. Miyake does not provide a detailed description of the cache operation of the embodiment of Figs. 35-37. (Col. 36, ll. 44- 53.) Miyake, however, does describe that in cache (normal) mode the operation of its configurable memory "is essentially the same as the operation of the conventional cache computer." (col. 36, ll. 49-53.) As explained throughout Miyake (e.g., Figs. 7-10, 12, 13, 15-22, 24, 25, and 27-30, and corresponding text), tags and corresponding data are included in each cache block. (Col. 25, ll. 51-55; Fig. 29). Similarly, the cache (memory) portion (320) includes tag data (307) corresponding to cache memory (326). (Col. 35, ll. 45-61; Fig. 37.)

18. Miyake describes the operation of the address comparison and control signal for the non-cache memory configuration as follows:

> [T]he CPU 310 accesses a certain address of the RAM. The address accessed by the CPU 310 is transferred to the comparator 347. The address accessed by the CPU 310 is compared with the RAM address (the RAM address space) sent by the RAM address register 345 at the comparator 347. The result of the comparison is sent from the comparator 347 to the RAM miss request unit 353.

> When a match between the accessed address and the stored RAM address occurs at the comparator 347, the RAM miss request unit 353 sends a cache hit signal (CH) to the bus control unit 328. At the same time, the RAM miss request unit 353 supplies a cache way select signal (CWS) to the selector 335 in accordance with the signal sent by the way setting flag 341. The selector 335 supplies a select signal to the data selection unit 313 in accordance with both the cache way select signal (CWS) sent by the RAM miss request unit 353 and the decoded address sent by the decoder 333. The data selection unit 313 supplies the selected data, output by the cache memory 326, to both the CPU 310 and the bus control unit 328.

(Col. 37, ll. 40-60; Figs. 37, 38.)

PRINCIPLES OF LAW

Burden on Appeal

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

Written Description

An applicant must "convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the [claimed] invention." *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991).

Anticipation

Anticipation is a question of fact. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997). Under 35 U.S.C. § 102, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987) (citations omitted); *see also Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005)(citation omitted).

ANALYSIS

Issue 1: Rejection of claim 29 under 35 U.S.C. § 112, first paragraph

Appellants contend that claim 29 complies with the written description requirement. (App. Br. 9-11.) The Examiner maintains Appellants' "specification does not support the claimed configurable memory with three modes of operation where any one of the modes is selectable at any time." (Ans. 4.) Accordingly, we decide the question of whether Appellants have shown error in the Examiner's finding that the claim fails to comply with the written description requirement– i.e., fails to convey with reasonable clarity to those skilled in the art, as of the filing date sought, that Appellants were in possession of the subject matter recited in the claim.

After reviewing the record on appeal, we find Appellants' Specification only describes two modes of configurable memory operation, a cache mode and a local, non-cache mode. (FF 1, 2.) Although the Specification ostensibly describes four separate modes of operation – a local memory read mode, a local memory write mode, a cache read mode, and a

cache write mode (FF 2) – these modes fall within either the cache or local (non-cache) modes. We agree with the Examiner that Appellants do not describe three modes of configurable memory operation.

> As explained by our reviewing court in the recent *Hyatt* case:
>
> Adequate written description means that, in the specification, the applicant must "convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the [claimed] invention." When no such description can be found in the specification, the only thing the PTO can reasonably be expected to do is to point out its nonexistence.

Hyatt v. Dudas, 492 F.3d 1365, 1370 (Fed. Cir. 2007) (internal citations omitted) (quoting *Vas-Cath*, 935 F.2d at 1563-64); (citing *In re Alton*, 76 F.3d 1168, 1175 (Fed. Cir. 1996)). Here, the Examiner has properly pointed out that the contested limitation is not disclosed by, and is therefore outside the scope of, the Specification.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's written description rejection of claim 29. Accordingly, we affirm the Examiner's rejection of the claim.

Issue 2: Rejection of claims 1-8 under 35 U.S.C. § 102(e) over Kumar

Kumar describes an integrated circuit (chip) with a configurable (reconfigurable) memory that operates as either on-chip main memory or as on-chip cache. (FF 4.) Kumar's configurable memory includes a tag array (memory array) and a data array (memory array). Each row of the tag array corresponds to a data line in the data array. (FF 5.) We find that an ordinarily-skilled artisan would have understood Kumar to disclose a

memory array storing both tag bits and data bits stored in a memory array, as recited in claim 1.

Appellants, however, contend that Kumar does not disclose a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation. (App. Br. 13.)

The Examiner maintains that Kumar discloses "there is a one-to-one correspondence between a tag and its corresponding data, forming a single logical line that comprises both tag and data." (Ans. 15.) Accordingly, we decide the question of whether Kumar discloses a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation.

We note at the outset, as a general proposition, merely reciting that data corresponds to a particular type of data, e.g., tag bits or data bits, as opposed to some other unique identifier, essentially constitutes non-functional descriptive material as it does not further limit the claimed invention either functionally or structurally. Such non-functional descriptive material does not patentably distinguish claims over the prior art that otherwise renders the claims unpatentable. *In re Ngai*, 367 F.3d 1336, 1339 (Fed. Cir. 2004).[4] Appellants' contested limitation merely requires a memory array storing data (two types of data – tag bits and data bits) in a data line in the memory array during cache operation. This feature is

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[4] *See also Ex parte Nehls*, 88 USPQ2d 1883, 1887-89 (BPAI 2008) (precedential) (discussing cases pertaining to non-functional descriptive material); *Ex parte Mathias*, 2005 WL 5121483 (BPAI Aug. 19, 2005), *aff'd* by *In re Mathias*, 2006 WL 2433879 (Fed. Cir. Aug. 17, 2006) (Rule 36, unpublished); *Ex parte Curry*, 84 USPQ2d 1272 (BPAI 2005) (informative), *aff'd by In re Curry*, No. 2006-1003 (Fed. Cir. 2006) (Rule 36, unpublished) (both cases treating data as nonfunctional descriptive material).

inherent in any cache memory. As we explain *infra*, the claim does not recite any function or structural relationship between the tag bits, the data bits, and the memory.

We initially note disagreement between the Examiner and the Appellants concerning the limitation of a "single data line in the memory array." We determine the scope of the claims in patent applications not solely based on the claim language, but upon giving claims "their broadest reasonable interpretation consistent with the specification" and "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted).

Appellants do not explicitly define a "memory or "memory array." Accordingly, we broadly construe a memory (memory array) as integrated circuits allowing storage and access to data. It is notoriously well known that memories may be constructed of multiple components and/or partitioned into separate portions – i.e., a memory may have multiple memory arrays or portions. Consistent with this interpretation, Appellants utilize the term memory and memory array interchangeably (e.g., "RAM memory array" having a "memory portion," memory array 130 (which includes additional control components) including memory array 410). (FF 1, 3.)

The "single data line" terminology appears conceptual, and is also not defined in Appellants' Specification. Although Appellants do not explicitly define a "data line," they do explain that the "configurable RAM array has a memory portion for storing tag bits and data bits in a single logical line." (FF 1.) Appellants also explain that cache tags may be "included in data lines stored in the memory array," or alternatively in separate memory

arrays. (FF 3.) We construe a "single data line" and "single logical line" simply as a line (string) of data. Accordingly, we construe a "single data line in the memory array" as a line of data within a memory or portion of memory.

After reviewing the record on appeal, we find Kumar discloses a memory (memory portion and/or memory array) storing both tag bits and data bits in a single line of data, as recited in claim 1. We agree with the Examiner that Kumar discloses storing the tag and its corresponding data in the memory array (tag array and data array) in a single logical line of data that comprises both tag bits and data bits. We also note that nothing in Appellants' claim precludes storing the tags and data in separate portions of the memory (memory array) – if the tag bits and data bits are stored in a manner directly corresponding with one another, as disclosed by Kumar, then the tags and data are stored in a single line of data.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's anticipation rejection of independent claim 1. Claims 2-8 depend from claim 1 and are not separately argued. Accordingly, we will affirm the Examiner's rejection of claims 1-8.

Issue 3: Rejection of claims 10-14 under 35 U.S.C. § 102(e) over Kumar

Kumar discloses a configurable memory capable of selecting either a first or a second operating mode (cache or main memory operating mode) based upon an address comparison – the reconfigurable memory examines (compares) an address supplied by the CPU, and outputs data in response to a valid address (either for cached data or main memory data) and a control signal. (FF 6, 7.)

In cache mode (cache configuration), Kumar's comparator circuit compares the tag bits from the address register to the tag bits from the tag array, and generates a cache hit signal if the tag bits match. (FF 8.) The tag bits represent a part of the address in the address register, i.e., a range of addresses. (FF 9.) The control circuit enables the data output in response to the control signal indicating a cache configuration and the cache hit. (FF 8.)

Similarly, in non-cache mode (main memory configuration), Kumar's comparator circuit compares a portion of the address from the address register to a base address. (FF 6, 10.) The control circuit enables the data output in response to the control signal indicating a main memory configuration and a valid address range. (FF 10.)

Appellants, however, contend that Kumar does not disclose that "the configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses" (App. Br. 15, claim 10) – i.e., a configurable memory that is capable of selecting (having selected) either the first or second mode of operation based upon an address comparison (to a range of addresses). Appellants also contend that the Examiner "seems to place no patentable weight" on the contested claim limitation. (App. Br. 15.)

The Examiner maintains that Kumar discloses the feature (i.e, the capability of having either the first or second mode of operation selected based upon an address comparison) (Ans. 6) – "Kumar's configurable memory is capable of responding to a control signal generated by address comparison so long as the generated signal is the same type of signal as the control signal 36." (Ans. 19.) Accordingly, we decide the question of

whether Kumar discloses a configurable memory that is capable of selecting either a first mode of operation or a second mode of operation based upon an address comparison.

After reviewing the record on appeal, we find Kumar discloses that its configurable memory is capable of selecting either a first mode of operation or a second mode of operation based upon an address comparison. We agree with the Examiner that Kumar's configurable memory responds to the signal generated by an address comparison, as well as the control signal 36. Thus, Kumar's configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of an address comparison (comparing a supplied address to a range of addresses), as recited in claim 10.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's anticipation rejection of claim 10. Claims 11-14 depend from claim 10 and are not separately argued. Accordingly, we will affirm the Examiner's rejection of claims 10-14.

Issue 4: Rejection of claims 1 and 21 under 35 U.S.C. § 102(e) over Saulsbury

Saulsbury discloses an integrated circuit with a memory configurable as either cache or non-cache memory. Saulsbury explains that the memory can be configured as either cache memory with associated tags, as directly accessible physical memory, and as a combination of both cache and physical memory. (FF 11, 12.)

As with Kumar (Issue 2), *supra*, Appellants contend that Saulsbury does not disclose a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache

operation. Specifically, Appellants contend that Saulsbury discloses separate caches for tags and data.

The Examiner maintains that Saulsbury discloses memory that can be configured as either cache memory with associated tags, or as directly accessible physical memory, and that the tag bits and data bits form a data line. (Ans. 18.) Accordingly, we decide the question of whether Saulsbury discloses a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation.

We initially note that Appellants' contention that Saulsbury discloses separate caches is inapposite to the Examiner's rejection, and is without merit. The caches referenced by Appellants relate to the processor core VLIW pipeline, not to the memory. (¶¶ [0017]-[0020], [0037]; Figs. 1, 3.)

After reviewing the record on appeal, we find Saulsbury discloses a memory storing both tag bits and data bits in a single line of data, as recited in claim 1. As explained with respect to issue 2, *supra*, the recitation of tag bits and data bits constitutes non-functional descriptive material that does not patentably distinguish this claim limitation. Saulsbury expressly discloses "cache memory with associated tags." (FF 12.) We agree with the Examiner, and we find this disclosure describes a memory storing tags and data in a data line in cache operation mode.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's anticipation rejection of independent claim 1. Claim 21 depends from claim 1 and is not separately argued. Accordingly, we will affirm the Examiner's rejection of claims 1 and 21.

Issue 5: Rejection of claims 1 and 21 under 35 U.S.C. § 102(e) over Baltz

Baltz discloses an integrated circuit with a configurable memory, and a program memory controller (PMC) that configures the memory as either cache or non-cache memory. The PMC includes data RAM (program memory/cache) and tag RAM. In cache mode, the PMC tag RAM stores tags corresponding to each frame of the memory. (FF 13, 14.)

After reviewing the record on appeal, we find Baltz discloses a memory storing both tag bits and data bits in a single line of data, as recited in claim 1. As explained with respect to issue 1, *supra*, the recitation of tag bits and data bits constitutes non-functional descriptive material that does not patentably distinguish this claim limitation. Also, as we explained *supra*, Appellants' claim does not preclude storing the tags and data in separate portions of the memory where the tag and data directly correspond with one another. Baltz discloses this correspondence. (FF 14.)

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's anticipation rejection of independent claim 1. Claim 21 depends from claim 1 and is not separately argued. Accordingly, we will affirm the Examiner's rejection of claims 1 and 21.

Issue 6: Rejection of claims 10-14 under 35 U.S.C. § 102(e) over Baltz

Baltz discloses a PMC which performs an address comparison in order to determine if valid data is stored in the on-chip memory. In memory map (non-cache) mode, the PMC determines if the provided address corresponds to a particular block of memory. In cache mode, the PMC compares a portion of the provided address with a tag to determine a cache

hit. The data from the requested address is then the valid data is retrieved from the memory. (FF 15.)

As with issue 3, *supra*, Appellants contend that: (1) Baltz does not disclose a configurable memory that is capable of selecting either the first or second mode of operation based upon an address comparison; and (2) the Examiner fails to ascribe patentable weight to the contested claim limitation. (App. Br. 18.)

The Examiner maintains that Baltz discloses the feature. (Ans. 9, 19.) Accordingly, we decide the question of whether Baltz discloses a configurable memory that is capable of selecting either a first mode of operation or a second mode of operation based upon an address comparison.

After reviewing the record on appeal, we agree with the Examiner, and we find Baltz discloses a configurable memory capable of selecting either a first or a second operating mode based upon an address comparison, as recited in claim 10.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's anticipation rejection of claim 10. Claims 11-14 depend from claim 10 and are not separately argued. Accordingly, we will affirm the Examiner's rejection of claims 10-14.

Issue 7: Rejection of claims 1-3, 6-10, 13-17, 20, and 21 under 35 U.S.C. § 102(e) over Miyake

Miyake discloses an integrated circuit with a memory configurable as either cache or non-cache memory. As with Kumar (Issue 2) and Baltz (Issue 5), *supra*, Miyake discloses that the memory (cache) includes tag data corresponding to cache memory. (FF 16, 17.)

As with Kumar (Issue 2) and Baltz (Issue 5), *supra*, Appellants contend that Miyake does not disclose a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation. (App. Br. 19.) Similarly, the Examiner maintains that Miyake discloses memory configurable as either cache memory with associated tags, or as local, non-cache memory, and that the tag bits and data bits form a data line. (Ans. 10, 18.) Accordingly, we decide the question of whether Miyake discloses a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation.

After reviewing the record on appeal, we find Miyake discloses a memory storing both tag bits and data bits in a single line of data, as recited in claim 1. As with Kumar (Issue 2) and Baltz (Issue 5), *supra*, the recitation of tag bits and data bits constitutes non-functional descriptive material that does not patentably distinguish this claim limitation. Miyake discloses tag data corresponding to cache memory in its memory (cache portion) (FF 17.) Thus, we agree with the Examiner, and we find Miyake discloses a memory storing tags and data in a data line in cache operation mode.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's anticipation rejection of independent claim 1. Claims 2, 3, 6-10, 13-17, 20, and 21 depend from claim 1 and are not separately argued. Accordingly, we will affirm the Examiner's rejection of claims 1-3, 6-10, 13-17, 20, and 21.

Issue 8: Rejection of claims 22, 23, 25, 26, 29, 30, 32, and 33 under 35 U.S.C. § 102(e) over Miyake

Miyake discloses an address comparison and control signal utilized in its memory's non-cache configuration. The CPU provides an address to the cache controller (325) that includes a comparator (347) and an address register (345). The comparator compares the provided address with address register, and when a match occurs a cache hit signal is produced. (FF 18.)

Appellants, contend that Miyake does not disclose "*comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select one of the modes of operation*, as generally recited in Claims 22, 26, 29, 30, and 33." (App. Br. 20.)

The Examiner maintains that Miyake discloses a configurable memory array having a first and a second mode of operation selectable based on comparing a supplied address to an address range contained in a configuration register and generating a control signal based on the comparison. (Ans. 10, 20-21.) Accordingly, we decide the question of whether Miyake discloses generating a control signal based on an address comparison of a supplied address to at least one address range contained in a configuration register to select the first or second mode of operation.

After reviewing the record on appeal, we find Miyake discloses generating a control signal based on an address comparison of a supplied address to an address range contained in a configuration register to select the first or second mode of operation, as recited in claims 22, 26, 29, 30, and 33. As with Kumar (Issue 2), *supra*, the recitation of an address range (data) in a configuration register (data register) constitutes non-functional descriptive material that does not patentably distinguish this claim limitation. We

construe the claim limitation as merely requiring comparison of an address to data in a register. Miyake discloses comparing a provided address to data (e.g., an address range) in a register (address register) and generating a signal (cache hit signal) from the address comparison. (FF 18.) Thus, we agree with the Examiner, and we find Miyake discloses generating a control signal based on an address comparison of a supplied address to at least one address range contained in a configuration register to select the first or second mode of operation.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's anticipation rejection of independent claims 22, 26, 29, 30, and 33. Claims 23, 25, and 32 depend from claims 22 and 30, respectively, and are not separately argued. Accordingly, we will affirm the Examiner's rejection of claims 22, 23, 25, 26, 29, 30, 32, and 33.

Rejection of claims 24, 27, 28, 31, and 34-37 under 35 U.S.C. § 103(a)

Appellants do not separately argue claims 24, 27, 28, 31, and 34-37. Accordingly, Appellants have not persuaded us of error in the Examiner's obviousness rejection of claims 24, 27, 28, 31, and 34-37, and we will affirm the Examiner's rejection of the claims.

CONCLUSION OF LAW

On the record before us, we find that Appellants have not established that the Examiner erred in finding: (1) Appellants fail to comply with the written description requirement; (2) Kumar, Saulsbury, Baltz, and Miyake disclose a configurable memory with a memory array storing both tag bits and data bits in a single data line in the memory array in cache operation; (3)

Kumar and Baltz disclose a configurable memory that is capable of selecting either the first mode of operation or the second mode of operation based upon an address comparison; and (4) Miyake discloses generating a control signal based on an address comparison of a supplied address to at least one address range contained in a configuration register to select the first or second mode of operation.

DECISION

We affirm the Examiner's rejection of claims 1-23, 25, 26, 29, 30, 32 and 33 under 35 U.S.C. § 102(e).

We affirm the Examiner's rejection of claims 24, 27, 28, 31, and 34-37 under 35 U.S.C. § 103(a).

AFFIRMED

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F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11797